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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,523	06/29/2001	Steven K. Hsu	884.453US1	8095

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EJC

Office Action Summary	Application No.	Applicant(s)	
	09/896,523	HSU ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 29-30, 31-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano (5,191,233) in view of Fujioka (5,559,996) and Avery et al (6,002,290).

Claims 29-31, Nakano shows a voltage-level converter (Fig. 2) comprising:

a static voltage-level converter including at most four transistors (P1, P2, N1, N2) and an inverter (a triangular shape) coupled to no more than two transistors in the static voltage-level converter each of the no more than two transistors directly coupled to a voltage level (GND); and

a split-level output circuit (P4 & N3) coupled to the static voltage-level converter, the split-level output circuit including a first split-level input node (the gate of P4) and a second split-level input nodes the second split-level input node directly coupled to an output of the inverter (the gate of N3), and the first split-level input node adapted to receive a complementary signal of the signal received at the second split-level input node:

wherein the static voltage-level converter comprises:

an input node (IN), a first output node, and a second output node (the gate of N3);

a first pair of transistors connected in series, the first pair of transistors including a first transistor (N1) and a second transistor (P1), the first transistor coupled to the input node; and

a second pair of transistors connected in series, the second pair of transistors including a first transistor (N2) and a second transistor (P2), the second transistor of the second pair of transistors being cross-coupled with the second transistor of the first pair of transistors (P1 and P2 is cross-coupled) and the second transistor of the second pair of transistors being coupled to the first output node, wherein the inverter is coupled to the input node, to the first transistor of the second pair of transistors, and to the second output node.

Nakano shows the claimed invention except for the second transistor of the first pair of transistors and the second transistor of the second pair of transistors are down-sized.

However, Fujioka teaches that is known to down-sized the cross-coupled P-channel transistors as set forth at column 8, lines19-50. Also, Avery teaches that is known to down-sized the cross-coupled P-channel transistors as set forth at column 2, lines 7-13.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to down-sized the cross-coupled P-channel transistors, as taught by Fujioka and Avery in order for the level shifter to work properly with minimal power consumption.

Claims 32-40, Figure 2 of Nakano shows all the limitations and the connection of the transistors, the inverter, and the split-level output circuit exactly of Applicant's invention figure 3B.

3. Claims 41-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano (5,191,233) in view of Fujioka (5,559,996) and Avery et al (6,002,290) further view of Tanaka et al (6,249,145).

Claims 41-48, Nakano in view of Fujioka and Avery disclose the claimed invention regarding a voltage level converter as described above in claims 29-40 except for first logic unit coupled to a first voltage level, a second logic unit coupled to a second voltage level that is greater than the first voltage level and a voltage level converter coupled to the first and the second logic units.

Tanaka shows first logic unit (601, Fig. 14) coupled to a first voltage level (VDD), a second logic unit (602) coupled to a second voltage level (VDDQ) that is greater than the first voltage level and a voltage level converter (6031) coupled to the first and the second logic units.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the voltage level converter of Nakano in view of Fujioka and Avery connected to a first logic unit having a first voltage level and a second logic unit having second voltage level that is greater than the first voltage level, in order to provide two or more logic units that are power by different respective supply voltages.

Claims 49-50, Tanaka discloses wherein the non-critical function unit is a memory (col. 9, lines 31-36).

Claims 51-52, Tanaka discloses wherein the critical function unit is a clock generation circuit (clock function, col. 9, lines 19-21).

Claims 51-52, Tanaka discloses wherein the first logic unit (601) includes one logic unit in a non-critical path, and the second logic unit includes one logic unit in a critical path (602, VDDQ is higher than VDD).

4. Claims 54-56, Nakano in view of Fujioka and Avery further view of Tanaka discloses the claimed invention except for first logic unit, a second logic unit, and level voltage converter are embedded in a cell phone. It would have been obvious to one having ordinary skill in the art at the time the invention was made to first first logic unit, a second logic unit, and level voltage converter embedded in a cell phone, since it was known in the art that the cell phone includes many logic circuits having different voltage levels, and level converter which are common in the cell phone and computer system in order to consume less power than they would consume if only includes high voltage level circuits.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

10/19/05